FSD210B, FSD200B

Green Mode Fairchild Power Switch (FPS™)

Features

- Single Chip 700V Sense FET Power Switch for 7DIP
- Precision Fixed Operating Frequency (134KHz)
- FSD210B Consumes Under 0.1W at 265VAC & No Load with Advanced Burst-Mode Operation
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lockout (UVLO) with Hysteresis
- Built-in Soft Start
- Frequency Modultation for EMI Reduction
- FSD200B Does Not Require an Auxiliary Bias Winding

Applications

- Charger & Adapter for Mobile Phone, PDA & MP3
- Auxiliary Power for White Goods, PC, C-TV & Monitor

Related Application Notes

- AN-4137, 4141, 4147(Flyback) / AN-4134(Forward) / AN-4138(Charger)

Description

Each product in the FSD2x0B (x for 0, 1) family consists of an integrated Pulse Width Modulator (PWM) and Sense FET, and is specifically designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. Both devices are integrated high voltage power switching regulators which combine an avalanche rugged Sense FET with a voltage mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSD2x0B devices reduce total component count, design size, weight while increasing efficiency, productivity, and system reliability. Both devices provide a basic platform that is well suited for the design of cost-effective flyback converters.

OUTPUT POWER TABLE				
PRODUCT	230VAC ±15%(3)		85-265VAC	
	Adapter(1)	Open Frame(2)	Adapter(1)	Open Frame(2)
FSD210B	5W	7W	4W	5W
FSD200B	5W	7W	4W	5W
FSD210BM	5W	7W	4W	5W
FSD200BM	5W	7W	4W	5W

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

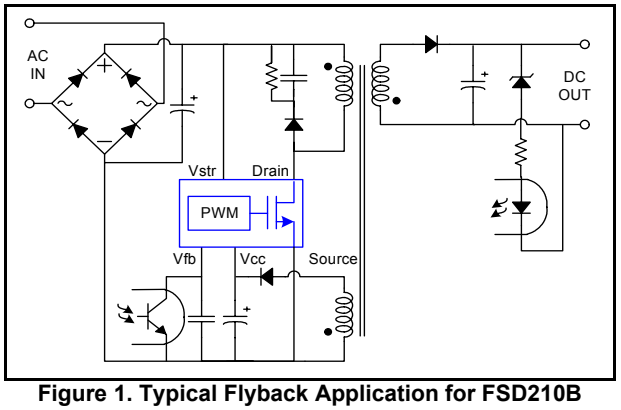


Figure 1. Typical Flyback Application for FSD210B

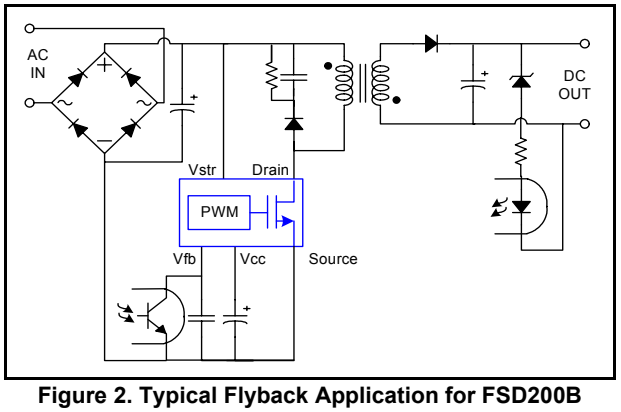


Figure 2. Typical Flyback Application for FSD200B

Internal Block Diagram

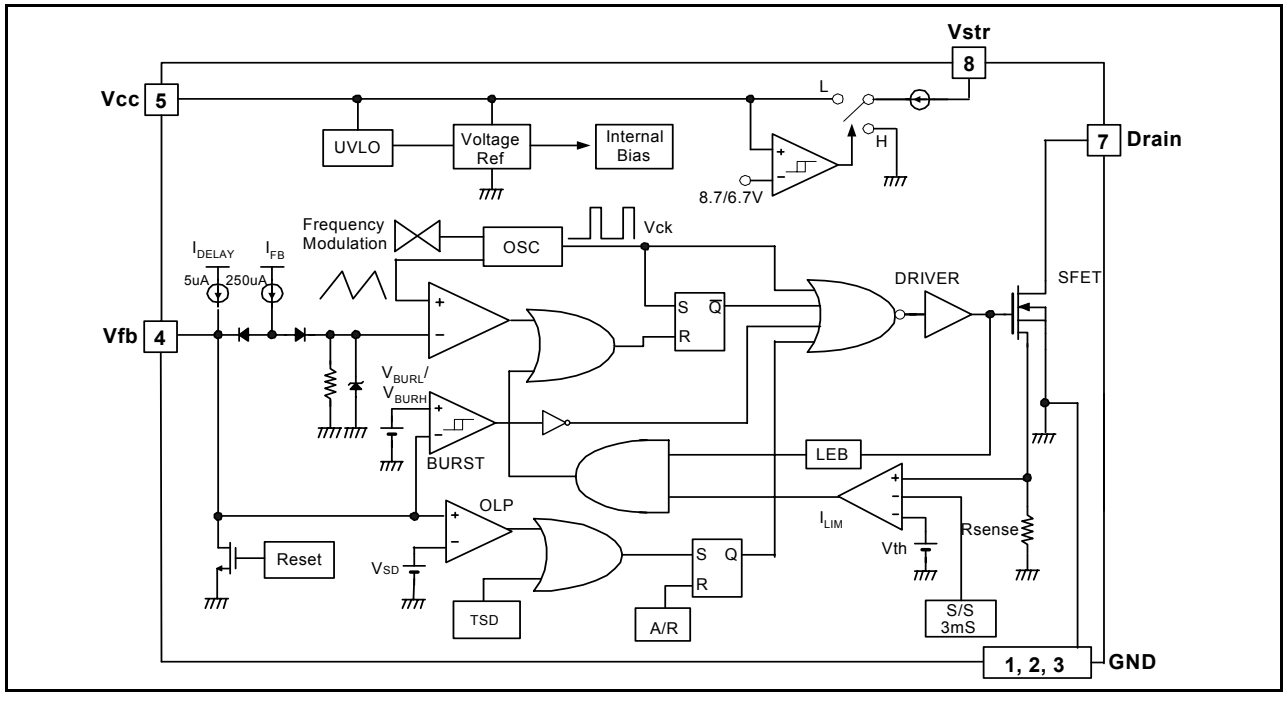


Figure 3. Functional Block Diagram of FSD210B

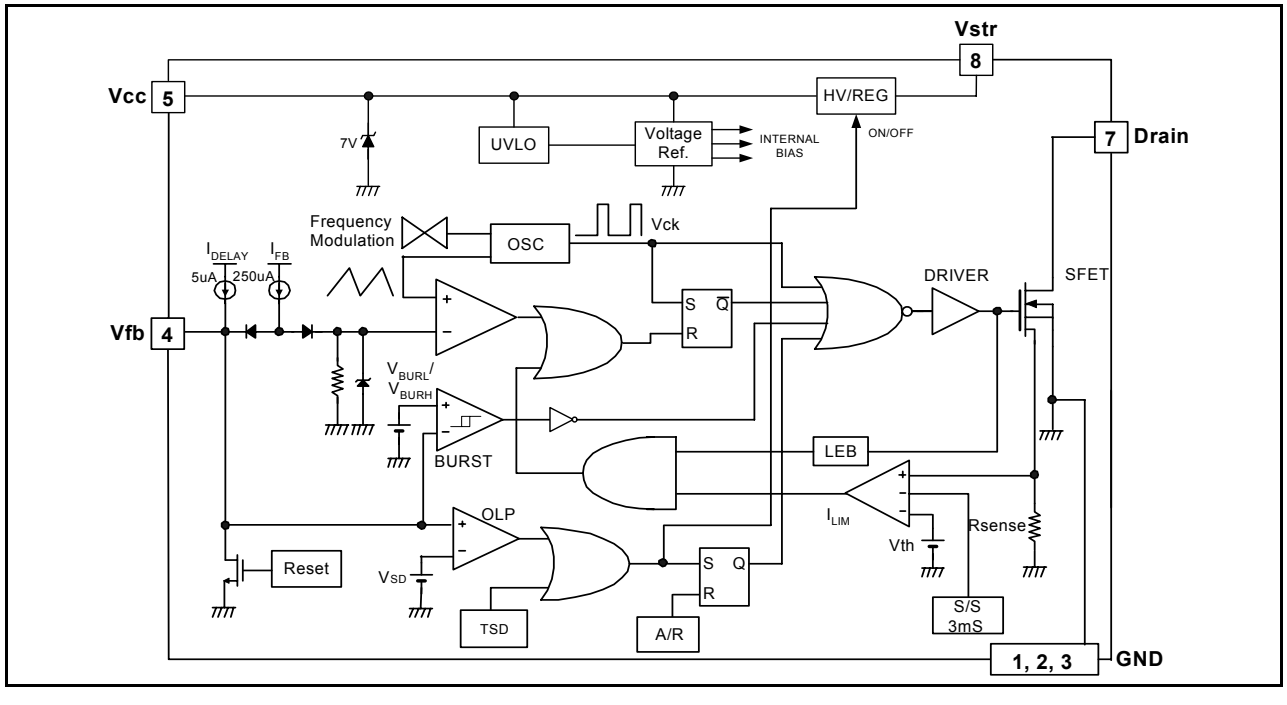


Figure 4. Functional Block Diagram of FSD200B

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1, 2, 3	GND	Sense FET source terminal on primary side and internal control ground.
4	Vfb	The feedback voltage pin is the inverting input to the PWM comparator and it has a normal input level between 0.5V and 2.5V. It has a 0.25mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 4.5V triggers over load protection (OLP). There is a time delay while charging external capacitor Cfb from 3V to 4.5V using an internal 5uA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
5	Vcc	**<FSD210B>** Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 8 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (8.7V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding. **<FSD200B>** This pin is connected to a storage capacitor. A high voltage regulator laid between pin 8 (Vstr) and this pin, provides supply voltage to the device during startup and normal operation. The FSD200B eliminates the need for an auxiliary bias winding and associated external components.
7	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 700V for 7DIP and 670V for 7LSOP. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.
8	Vstr	This pin connects directly to the rectified AC line voltage source for both the FSD200B and FSD210B. For the **FSD210B**, at start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 8.7V, the internal switch is opened. For the **FSD200B**, an internal high voltage regulator provides constant supply voltage.

Pin Configuration

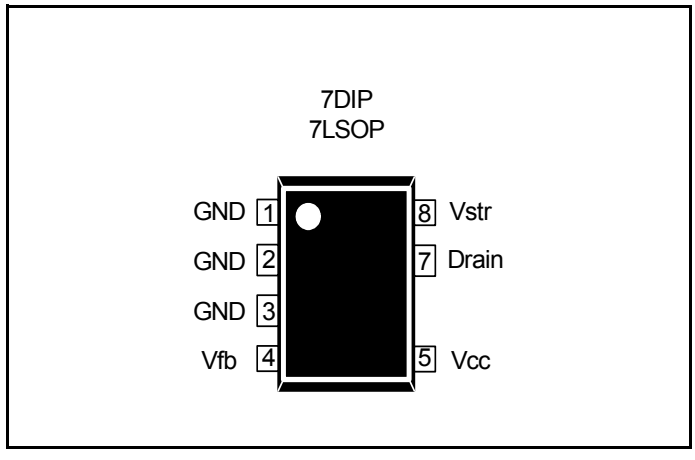


Figure 5. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Characteristic		Symbol	Value	Unit
Drain Pin Voltage	7DIP	V_{DRAIN}	700	V
Vstr Pin Voltage		V_{STR}	700	V
Total Power Dissipation		P_D	1.68	W
Drain Pin Voltage	7LSOP	V_{DRAIN}	670	V
Vstr Pin Voltage		V_{STR}	670	V
Total Power Dissipation		P_D	1.45	W
Supply Voltage	FSD200B	V_{CC}	10	V
Feedback Voltage Range		V_{FB}	-0.3 to V_{CC}	V
Supply Voltage	FSD210B	V_{CC}	20	V
Feedback Voltage Range		V_{FB}	-0.3 to V_{STOP}	V
Operating Junction Temperature		T_J	Internally limited	°C
Operating Ambient Temperature		T_A	-25 to +85	°C
Storage Temperature		T_{STG}	-55 to +150	°C

Thermal Impedance

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
7DIP			
Junction-to-Ambient Thermal(1)	θ_{JA}(3)	74.07	°C/W
	θ_{JA}(4)	60.44	°C/W
Junction-to-Case Thermal(2)	θ_{JC}	22.00	°C/W
7LSOP			
Junction-to-Ambient Thermal(1)	θ_{JA}(5)	86.02	°C/W
Junction-to-Case Thermal(2)	θ_{JC}	27.72	°C/W

Note:

1. Free standing with no heatsink. / Measurement Condition : Just before junction temperature T_J enters into OTP.
2. Measured on the DRAIN pin close to plastic interface.
3. Soldered to 100mm^2 copper clad.
4. Soldered to 300mm^2 copper clad.
5. Without copper clad.

- all items are tested with the standards JESD 51-2, 51-3 (SOP) and 51-10 (DIP).

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SENSE FET SECTION						
Zero-Gate-Voltage Drain Current	I_{DSS}	V_{DS}=560V, V_{GS}=0V	-	-	100	μA
Drain-Source On-State Resistance	$R_{DS(ON)}$	Tj=25°C, I_D=25mA	-	28	32	Ω
		Tj=100°C, I_D=25mA	-	42	48	
Rise Time	t_r	V_{DS}=325V, I_D=50mA	-	100	-	ns
Fall Time	t_f	V_{DS}=325V, I_D=25mA	-	50	-	ns
CONTROL SECTION						
Switching Frequency	f_{OSC}	Tj=25°C	126	134	142	KHz
Switching Frequency Modulation Range	Δf_{MOD}	Tj=25°C	-	±4	-	KHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=3.5V	60	66	72	%
Minimum Duty Cycle	D_{MIN}	V_{FB}=GND	0	0	0	%
UVLO Threshold Voltage **(FSD200B)**	V_{START}		6.3	7	7.7	V
	V_{STOP}	After turn on	5.3	6	6.7	V
UVLO Threshold Voltage **(FSD210B)**	V_{START}		8.0	8.7	9.4	V
	V_{STOP}	After turn on	6.0	6.7	7.4	V
Feedback Source Current	I_{FB}	V_{FB}=GND	0.22	0.25	0.28	mA
Internal Soft Start Time	$t_{S/S}$		-	3	-	ms
BURST MODE SECTION						
Burst Mode Voltage	V_{BURH}	Tj=25°C	0.58	0.64	0.7	V
	V_{BURL}		0.5	0.58	0.64	V
	$V_{BUR(HYS)}$	Hysteresis	-	60	-	mV
PROTECTION SECTION						
Peak Current Limit	I_{LIM}	$\Delta i/\Delta t$=150mA/us	0.275	0.320	0.365	A
Current Limit Delay Time(1)	t_{CLD}	Tj=25°C	-	220	-	ns
Thermal Shutdown Temperature(1)	T_{SD}		125	145	160	°C
Shutdown Feedback Voltage	V_{SD}		4.0	4.5	5.0	V
Leading Edge Blanking Time(2)	t_{LEB}		200	-	-	ns
Shutdown Delay Current	I_{DELAY}	V_{FB}=4.0V	3	5	7	μA
TOTAL DEVICE SECTION						
Operating Supply Current **(FSD200B)**	I_{OP}	(control part only),V_{CC}=7V	-	600	-	μA
Start-Up Charging Current **(FSD200B)**	I_{CH}	V_{CC}=0V	-	1	1.2	mA
Operating Supply Current **(FSD210B)**	I_{OP}	(control part only),V_{CC}=11V	-	700	-	μA
Start-Up Charging Current **(FSD210B)**	I_{CH}	V_{CC}=0V	-	700	900	μA
Vstr Supply Voltage	V_{STR}	V_{CC}=0V	20	-	-	V
Vcc Regulation Voltage **(FSD200B)**	V_{CCREG}		-	7	-	V

Note:

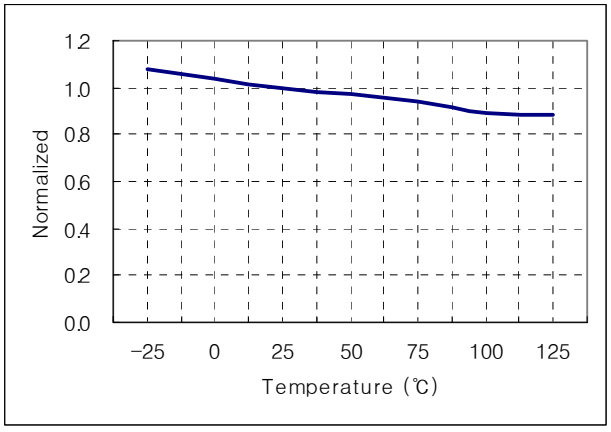
1. These parameters, although guaranteed, are not 100% tested in production
2. These parameter is derived from characterization

Comparison Between FSDH565 and FSD210B

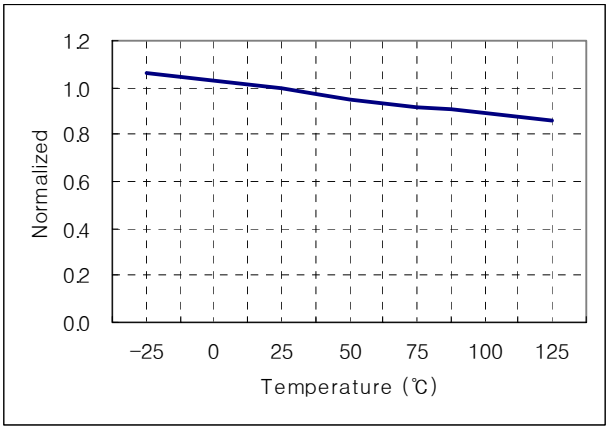
Function	FSDH565	FSD210B	FSD210B Advantages
Soft-Start	not applicable	3ms	• Gradually increasing current limit during soft-start further reduces peak current and voltage stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Switching Frequency	100KHz	134KHz	• Smaller transformer
Frequency Modulation	not applicable	± 4KHz	• Reduced conducted EMI
Burst Mode Operation	not applicable	Built into controller	• Improves light load efficiency • Reduces power consumption at no-load • Transformer audible noise reduction
Drain Creepage at Package	1.02mm	3.56mm DIP 3.56mm LSOP	• Greater immunity to arcing provoked by dust, debris and other contaminants

Typical Performance Characteristics (Control Part)

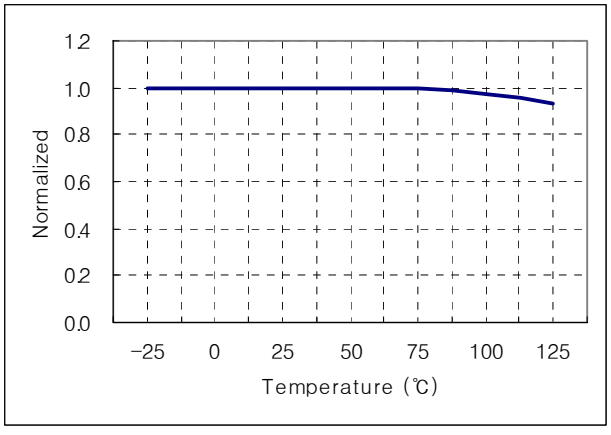
(These characteristic graphs are normalized at Ta = 25°C)



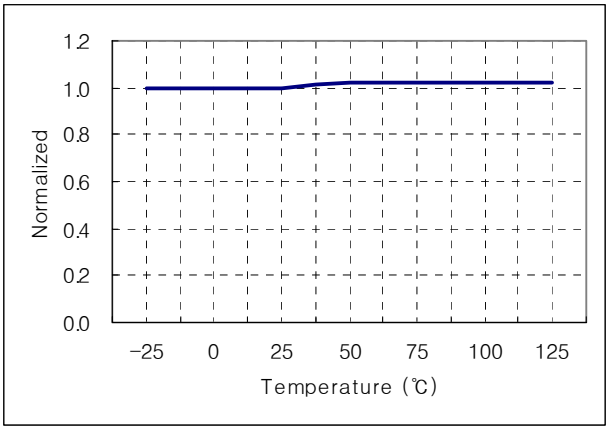
Switching Frequency (f_{OSC}) vs. Ta



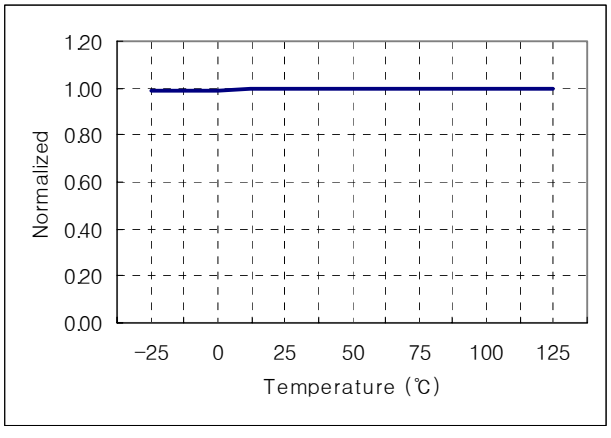
Operating Supply Current (I_{OP}) vs. Ta



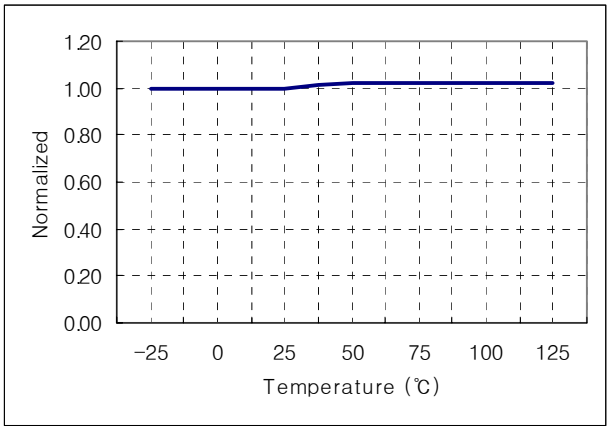
Peak Current Limit (I_{LIM}) vs. Ta



Feedback Source Current (I_{FB}) vs. Ta

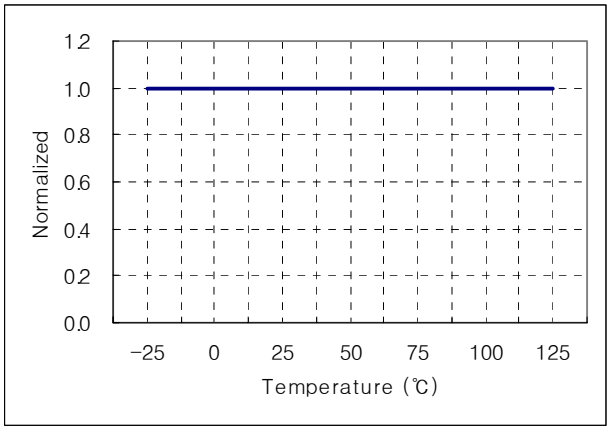


Start Threshold Voltage (V_{START}) vs. Ta

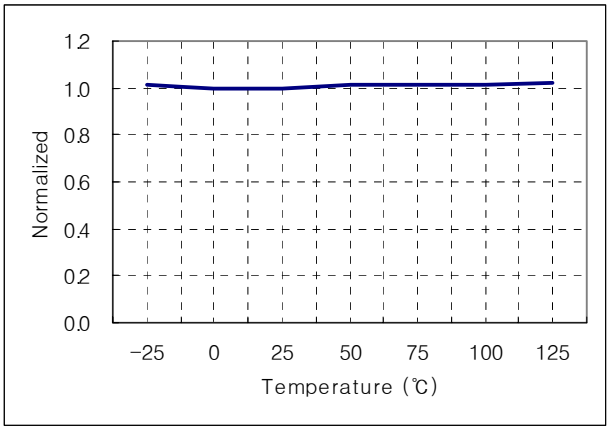


Stop Threshold Voltage (V_{STOP}) vs. Ta

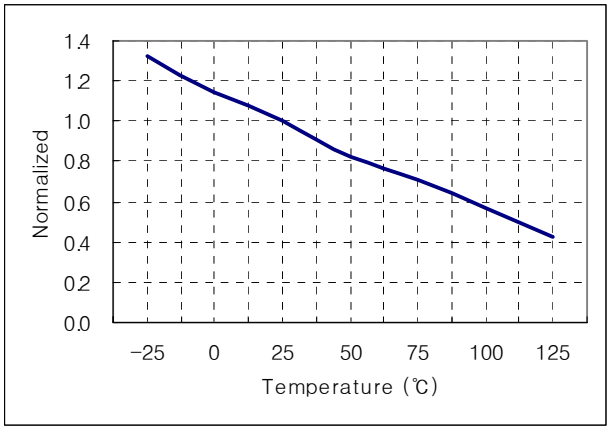
Typical Performance Characteristics (Continued)



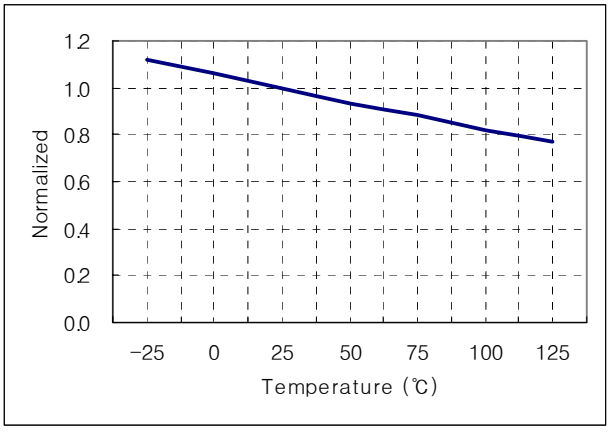
Vcc Regulation Voltage vs. Ta (for FSD200B)



Shutdown Feedback Voltage (V_{SD}) vs. Ta



Start Up Charging Current (I_{CH}) vs. Ta (for FSD210B)



Start Up Charging Current (I_{CH}) vs. Ta (for FSD200B)

Functional Description

1. Startup : At startup, the internal high voltage current source supplies the internal bias and charges the external Vcc capacitor as shown in Figure 7. In the case of the FSD210B, when Vcc reaches 8.7V the device starts switching and the internal high voltage current source is disabled. The device is in normal operation provided that Vcc does not drop below 6.7V. After startup the bias is supplied from the auxiliary transformer winding. In the case of FSD200B, An internal high voltage regulator (HV Req.) located between Vstr pin and Vcc pin regulates the Vcc to be 7V and supplies operating current, thus FSD200B needs no auxiliary bias winding.

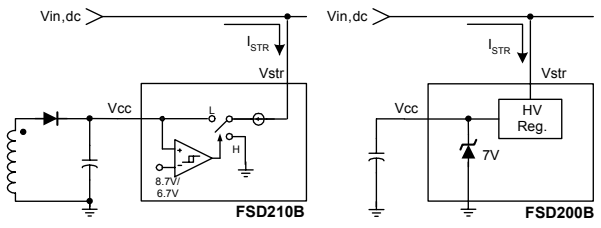


Figure 6. Internal Startup Circuit

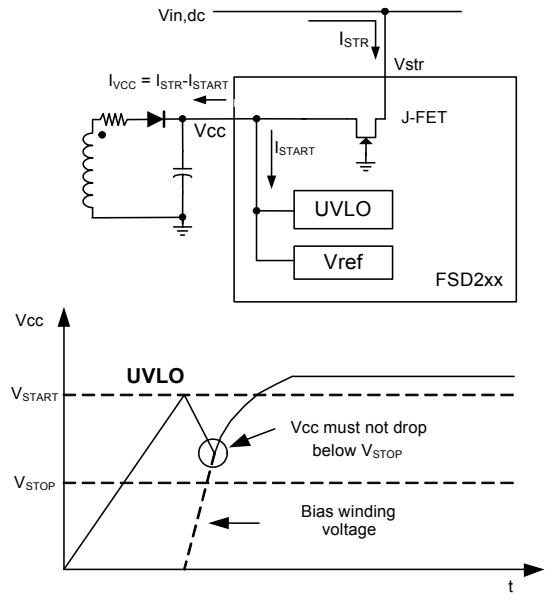


Figure 7. Charging Vcc Capacitor through Vstr

Calculating the Vcc capacitor is an important step to design with the FSD200B/210B. At initial start-up in the both devices, the maximum value of start operating current I_{START} is about 100uA, which supplies current to UVLO and Vref Blocks. The charging current I_{Vcc} of the Vcc capacitor is equal to I_{STR} - 100uA. After Vcc reaches the UVLO start voltage only the bias winding supplies Vcc current to device. When the bias winding voltage is not sufficient, the Vcc level decreases to the UVLO stop voltage. At this time Vcc oscillates. In order to prevent this oscillation it is recommended that the Vcc capacitor be chosen to have the value between 10uF and 47uF.

2. Feedback Control : The FSD200B/210B are voltage mode controlled devices as shown in Figure 8. Usually, an opto-coupler and KA431 type voltage reference are used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform. This directly controls the duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the optocoupler LED current increases, the feedback voltage Vfb is pulled down and it reduces the duty cycle. This will happen when the input voltage increases or the output load decreases.

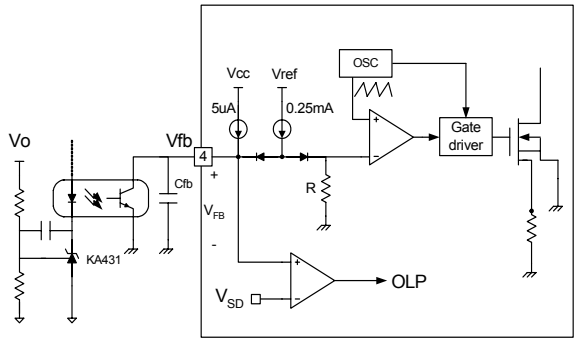


Figure 8. PWM and Feedback Circuit

3. Leading Edge Blanking (LEB) : At the instant the internal Sense FET is turned on, the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the Sense FET. Excessive voltage across the Rsense resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuit : The FSD200B/210B have 2 self-protection functions : over load protection (OLP) and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage V_{STOP} (6.7V-FSD210B, 6V-FSD200B), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage V_{START} (8.7V-FSD210B, 7V-FSD200B), the device resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

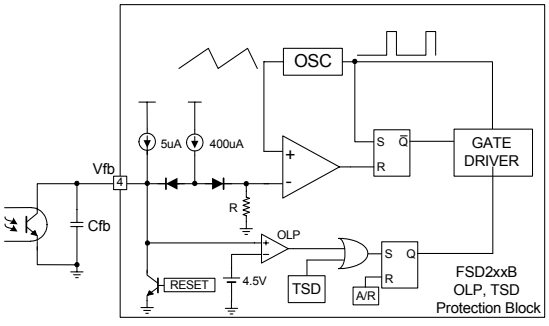


Figure 9. Protection Block

4.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the over load protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (Vo) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5uA current source (I_{DELAY}) starts to charge Cfb slowly up to Vcc. In this condition, V_{FB} increases until it reaches 4.5V, when the switching operation is terminated as shown in Figure 10. The shutdown delay time is the time required to charge Cfb from 3V to 4.5V with 5uA current source.

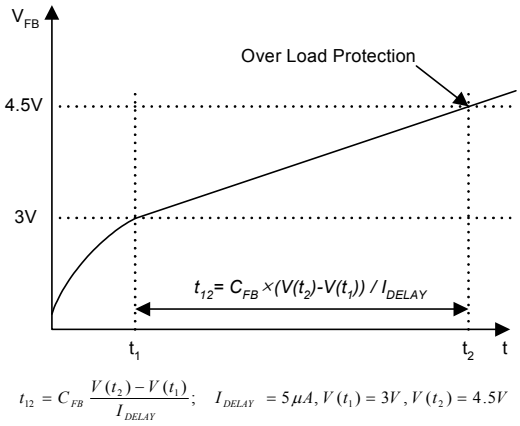


Figure 10. Over Load Protection (OLP)

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

5. Soft Start : FSD200B/210B has an internal soft start circuit that gradually increases current through the Sense FET as shown in Figure 11. The soft start time is 3msec in FSD200B/210B.

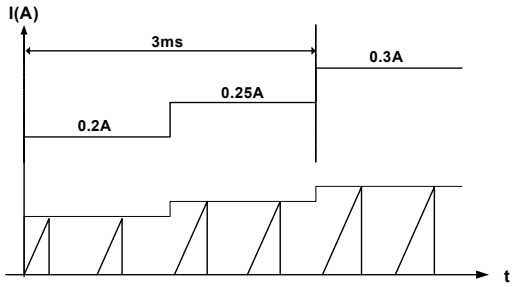


Figure 11. Internal Soft Start

6. Burst operation : In order to minimize the power dissipation in standby mode, the FSD200B/210B enter burst mode operation. As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below V_{BURL}(0.58V). At this point switching stops and the output voltages start to drop. This causes the feedback voltage to rise. Once is passes V_{BURH}(0.64V) switching starts again. The feedback voltage falls and the process repeats. Burst mode operation alternately enables and disables switching of the power MOSFET to reduce the switching loss in the standby mode.

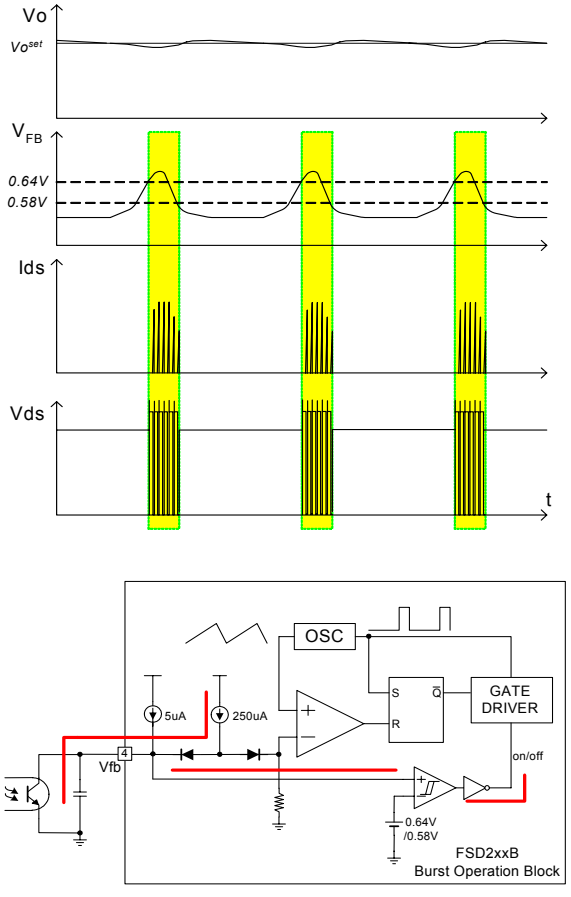


Figure 12. Burst Operation Function

7. Frequency Modulation : Modulating the switching frequency of a switched power supply can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 13, the frequency changes from 130KHz to 138KHz in 4ms for the FSD200B/210B. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

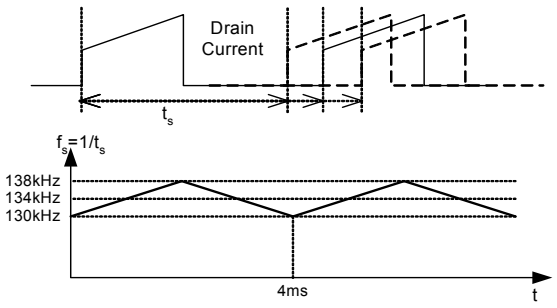


Figure 13. Frequency Modulation Waveform

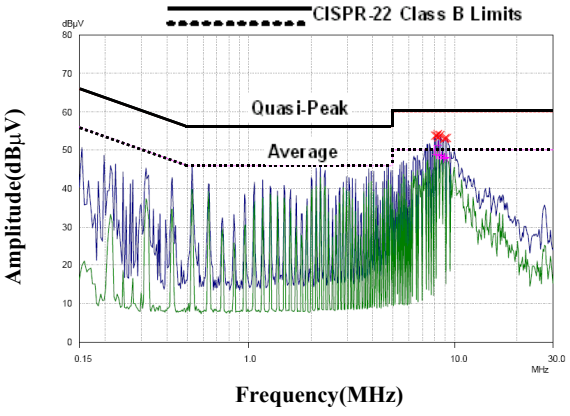


Figure 14. FSDH0165 Full Range EMI scan(100kHz, no Frequency Modulation) with charger set

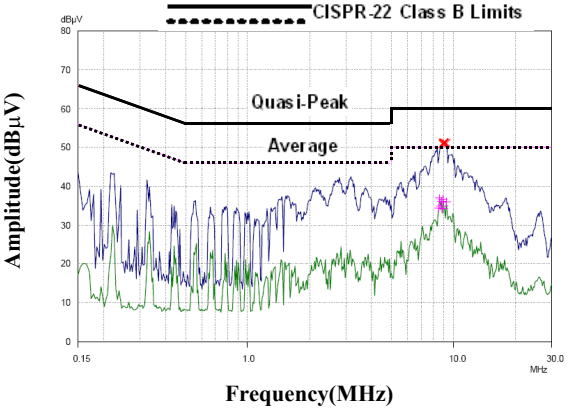


Figure 15. FSD210B Full Range EMI scan(134kHz, with Frequency Modulation) with charger set

Application Tips

1. Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000 Hz. Even though they operate above 20 kHz, they can make noise depending on the load condition. Designers can employ several methods to reduce these noises. Here are three of these methods:

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. But, it also can crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is considerable to use a zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4 kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4 kHz. When the fundamental frequency of noise is located in this range, one perceives the noise as louder although the noise intensity level is identical. Refer to Figure 16. Equal Loudness Curves.

When FPS acts in Burst mode and the Burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of Burst mode operation lies in the range of 2~4 kHz, adjusting feedback loop can shift the Burst operation frequency. In order to reduce the Burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D) and feedback capacitor (C_B) and decrease a feedback gain resistor (R_F) as shown in Figure 17. Typical Feedback Network of FPS.

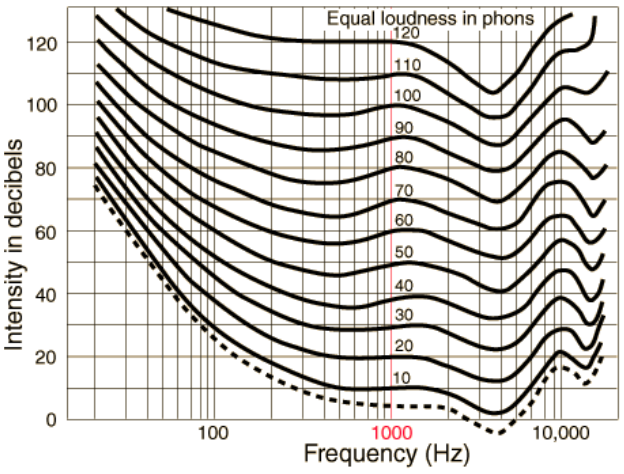


Figure 16. Equal Loudness Curves

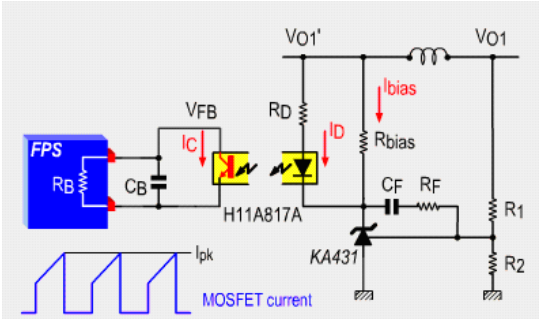


Figure 17. Typical Feedback Network of FPS

2. Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)

AN-4138: Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch (FPS™)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS Applications

Typical Application Circuit - 1

Application	Output power	Input voltage	Output voltage (Max current)
Cellular Phone Charger	3.38W	Universal input (85-265Vac)	5.2V (650mA)

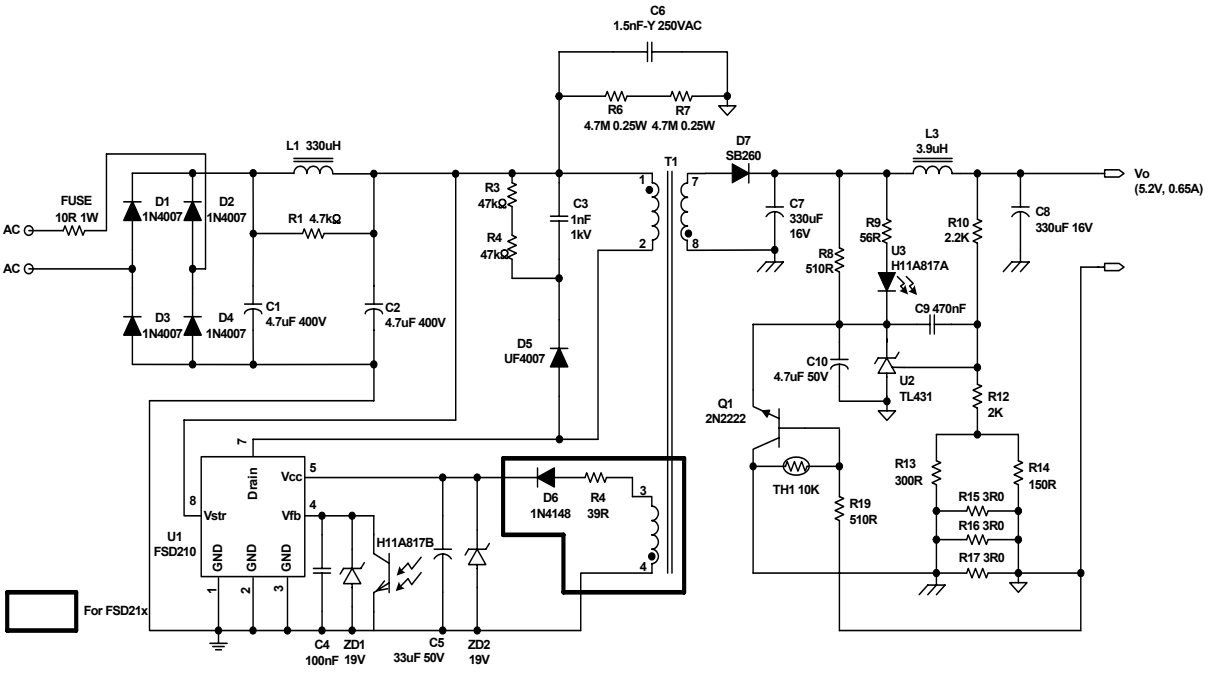
Features

- High efficiency (>67% at Universal Input)
- Low zero load power consumption (<100mW at 240Vac) with FSD210B
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (3ms)
- Frequency Modulation for low EMI

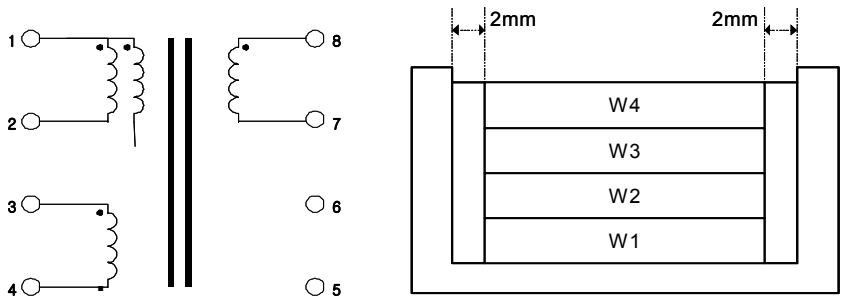
Key Design Notes

- The constant voltage (CV) mode control is implemented with resistors R8, R9, R10 and R11, shunt regulator U2, feedback capacitor C9 and opto-coupler U3.
- The constant current (CC) mode control is designed with resistors R8, R9, R15, R16, R17 and R19, NPN transistor Q1 and NTC TH1. When the voltage across current sensing resistors R15,R16 and R17 is 0.7V, the NPN transistor turns on and the current through the opto coupler LED increases. This reduces the feedback voltage and duty ratio. Therefore, the output voltage decreases and the output current is regulated.
- The NTC(negative thermal coefficient) resistor is used to compensate the temperature characteristics of the transistor Q1.
- The zener diodes (ZD1, ZD2) are used to bypass the ESD or surge.

1. Schematic



2. Transformer Schematic Diagram



CORE : EE1616

3. Winding Specification

	Pin(S → F)	Wire	Turns	Winding Method
W1	1 → 2	0.16φ×1	99	Solenoid winding
Insulation : Polyester Tape t = 0.025mm, 2Layers				
W2	4 → 3	0.16φ×1	18	Center Solenoid winding
Insulation : Polyester Tape t = 0.025mm, 2Layers				
W3	1 → open	0.16φ×1	50	Solenoid winding
Insulation : Polyester Tape t = 0.025mm, 3Layers				
W4	8 → 7	0.40φ×1	9	Solenoid winding
Insulation : Polyester Tape t = 0.025mm, 3Layers				

4. Electrical Characteristics

	Pin	Spec.	Remark
Inductance	1 - 2	1.6 mH	1kHz, 1V
Leakage	1 - 2	50 uH	3,4,7,8 short 100KHz, 1V

5. Core & Bobbin

Core : EER1616
Bobbin : EER1616

Typical Application Circuit - 2

Application	Output power	Input voltage	Output voltage (Max current)
Non-Isolation Buck	1.2W	DC 120 ~ 375V (for Universal Input)	12V (100mA)

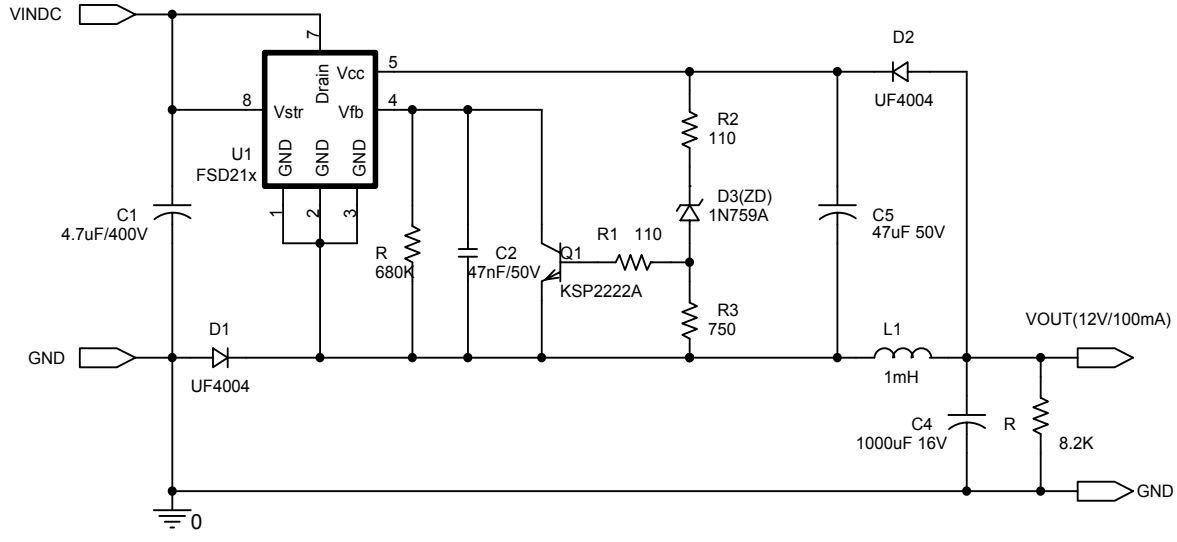
Features

- Non-Isolation Buck converter
- Low component count
- Enhanced system reliability through various protection functions

Key Design Notes

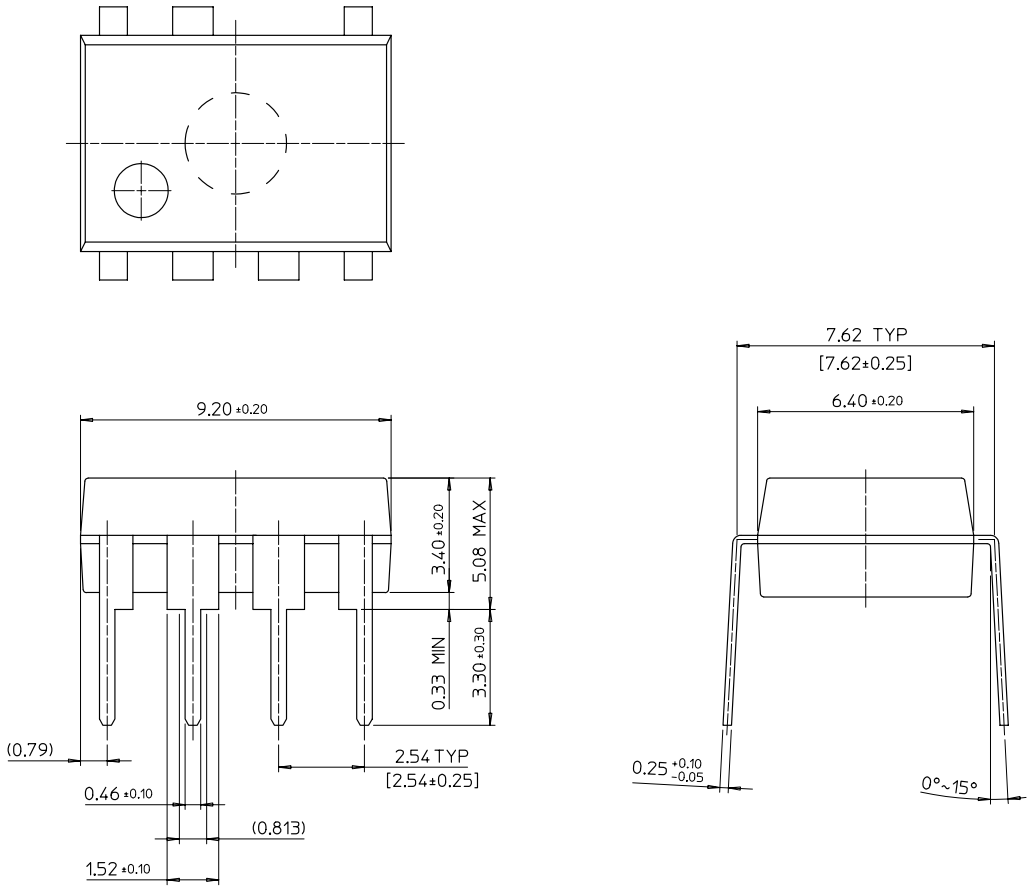
- The output voltage(12V) is regulated with resistors R1, R2 and R3, zener diode D3, the transistor Q1 and the capacitor C2. While the FSD210B is off, diodes D1 and D2 are on. At this time the output voltage 12V is sensed by the feedback components listed above.
- R 680K is used to prevent the OLP(over load protection) at startup.
- R 8.2K is a dummy resistor to regulate output voltage in light load.

1. Schematic



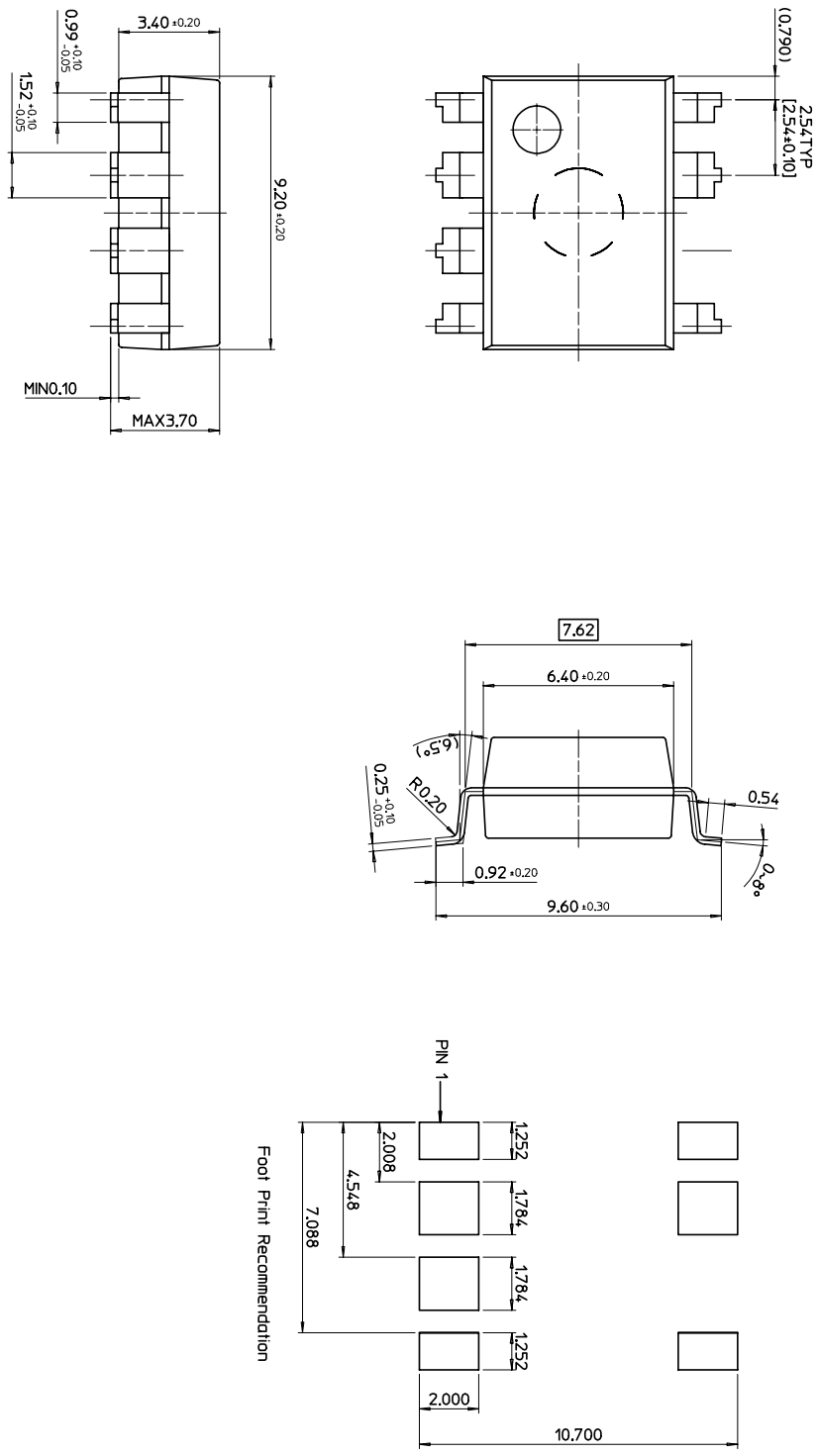
Package Dimensions

7-DIP



Package Dimensions (Continued)

7-LSOP



Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)}$
FSD210B	7DIP	FSD210	700V	134KHz	28Ω
FSD200B	7DIP	FSD200	700V	134KHz	28Ω
FSD210BM	7LSOP	FSD210	650V	134KHz	28Ω
FSD200BM	7LSOP	FSD200	650V	134KHz	28Ω